

What is claimed is:

1 1. A multilayer board, comprising  
2 a signal line requiring tamper-resistance, the signal line  
3 including: (a) a conductive trace and (b) a conductive via that  
4 passes through layers of the multilayer board, wherein  
5 the conductive trace and an end of the conductive via  
6 existing on an outside layer of the multilayer board are placed  
7 under one or more circuit components mounted on the outside layer.

1 2. The multilayer board of Claim 1, wherein  
2 the signal line further includes a conductive trace on  
3 an inner layer that is sandwiched between sheets of foil and/or  
4 circuit components placed on layers above and below the inner  
5 layer so that the sheets of foil and/or circuit components hide  
6 the conductive trace on the inner layer when viewed from above  
7 or below.

1 3. The multilayer board of Claim 2, wherein  
2 the sheets of foil placed on the layers that are outside  
3 the inner layer are connected to either a ground or a power source.

1 4. The multilayer board of Claim 3, wherein

2 the conductive trace on the outside layer is further  
3 covered by a circuit component on another outside layer when  
4 viewed from above or below.

1 5. The multilayer board of Claim 2, wherein  
2 the signal line requiring tamper-resistance is either a  
3 signal line that is input to an encryption unit or a signal line  
4 that is output from a decryption unit.

1 6. A multilayer board, comprising:  
2 a certain signal line that includes (a) a conductive trace  
3 and (b) a conductive via that passes through layers of the  
4 multilayer board, wherein  
5 the conductive trace and an end of the conductive via  
6 existing on an outside layer of the multilayer board are placed  
7 under one or more circuit components mounted on the outside layer,  
8 the certain signal line further includes a conductive trace  
9 on an inner layer that is sandwiched between sheets of foil and/or  
10 circuit components placed on layers above and below the inner  
11 layer so that the sheets of foil and/or circuit components hide  
12 the conductive trace on the inner layer when viewed from above  
13 or below, and  
14 the certain signal line is either a data line or an address

15 line.

1 7. A design apparatus for a multilayer board, the design  
2 apparatus comprising:

3 a component information acquiring means for acquiring  
4 component information that shows (a) positions of circuit  
5 components, (b) sizes of the components, and (c) terminals  
6 contained by the components;

7 a tamper-resistant signal line specifying means for  
8 specifying a signal line that requires tamper-resistance, among  
9 signal lines connecting terminals;

10 an outside layer wiring setting means for referring to  
11 the component information and setting areas on outside layers  
12 covered by circuit components as outside layer wiring possible  
13 areas;

14 a via setting means for referring to the component  
15 information, detecting an area where a first outside area wiring  
16 possible area of one outside layer overlaps another outside area  
17 wiring possible area of a second outside layer that is opposite  
18 to the first outside layer, when viewed from above or below in  
19 a vertical direction, and sets the detected area as a via possible  
20 area; and

21 a wiring information generating means for determining a

22 wiring pattern so that signal lines requiring tamper-resistance  
23 are wired only in the outside layer wiring possible areas and  
24 the via possible area, and generating wiring information that  
25 shows the determined wiring pattern.

1 8. The design apparatus of Claim 7 further comprising  
2 an inside layer wiring setting means for referring to the  
3 component information, detecting an area where a first outside  
4 area wiring possible area of one outside layer overlaps another  
5 outside area wiring possible area of a second outside layer that  
6 is opposite to the first outside layer, when viewed from above  
7 or below in a vertical direction, and sets the detected area  
8 as an inside layer wiring possible area, wherein  
9 the wiring information generating means determines the  
10 wiring pattern so that signal lines requiring tamper-resistance  
11 are wired only in the outside layer wiring possible areas, the  
12 via possible areas, and the inside layer wiring possible area,  
13 and generates the wiring information that shows the determined  
14 wiring pattern.

1 9. The design apparatus of Claim 8 further comprising  
2 an opposite layer wiring setting means for referring to  
3 the component information and setting areas on one outside layer

4 covered by components as opposite layer wiring possible areas,  
5 wherein

6 the wiring information generating means determines the  
7 wiring pattern so that signal lines requiring tamper-resistance  
8 are wired in areas on another outside layer that is opposite  
9 to the outside layer, the areas on the other outside layer  
10 overlapping the opposite layer wiring possible areas when viewed  
11 from above or below in a vertical direction.

1 10. A design apparatus for a multilayer board, the design  
2 apparatus comprising:

3 a board information acquiring means for acquiring board  
4 information that shows (a) the number of layers and (b)  
5 ground/power-source layers;

6 a tamper-resistant signal line specifying means for  
7 specifying a signal line that requires tamper-resistance;

8 an inside layer wiring setting means for referring to the  
9 board information and setting layers sandwiched between two  
10 ground/power-source layers as wiring possible inside layers;  
11 and

12 a wiring information generating means for determining a  
13 wiring pattern so that signal lines requiring tamper-resistance  
14 are wired in the wiring possible inside layers, and generating

15 wiring information that shows the determined wiring pattern.

1 11. A design apparatus for a multilayer board, the design  
2 apparatus comprising:

3 a board information acquiring means for acquiring board  
4 information that shows (a) wiring of signal lines that require  
5 tamper-resistance and (b) positions of components connected to  
6 the signal lines;

7 an exposed portion detecting means for referring to the  
8 board information and detecting portions of the signal lines  
9 that are not covered by the components connected to the signal  
10 lines on outside layers; and

11 a placement information generating means for determining  
12 a placement pattern so that one or more components that have  
13 not been placed yet are placed to cover the detected portions,  
14 and generating placement information that shows the determined  
15 placement pattern.

1 12. The design apparatus of Claim 11 further comprising  
2 an inside layer wiring detecting means for detecting  
3 portions of the signal lines wired on inside layers which are  
4 not sandwiched by the components on the outside layers when viewed  
5 from above or below in a vertical direction, wherein

6 the placement information generating means determines the  
7 placement pattern so that one or more components on one or more  
8 outside layers that have not been placed yet are placed to cover  
9 the portions detected by the inside layer wiring detecting means  
10 when viewed from above or below, and generates the placement  
11 information that shows the determined placement pattern.

1 13. The design apparatus of Claim 12 further comprising  
2 an opposite layer exposed portion detecting means for  
3 referring to the board information and detecting portions of  
4 the signal lines that are wired on one outside layer and are  
5 not covered by components connected to the signal lines on another  
6 outside layer that is opposite to the outside layer, wherein  
7 the placement information generating means determines the  
8 placement pattern so that one or more components on the opposite  
9 outside layer that have not been placed yet are placed to cover  
10 the portions detected by the opposite layer exposed portion  
11 detecting means when viewed from above or below, and generates  
12 the placement information that shows the determined placement  
13 pattern.

1 14. A design apparatus for a multilayer board, the design  
2 apparatus comprising:

3 a board information acquiring means for acquiring board  
4 information that shows (a) the number of layers and (b) wiring  
5 of signal lines;

6 a tamper-resistant signal line specifying means for  
7 specifying a signal line that requires tamper-resistance;

8 a plane layer detecting means for detecting, as plane  
9 layers, two layers that sandwich a layer on which the signal  
10 line is wired; and

11 a placement information generating means for determining  
12 a placement pattern so that sheets of foil on the plane layers  
13 cover the wiring of the signal line sandwiched by the plane layers  
14 when viewed from above or below in a vertical direction, and  
15 generating placement information that shows the determined  
16 placement pattern.

1 15. A design check apparatus for a multilayer board, the  
2 design check apparatus comprising:

3 a board information acquiring means for acquiring board  
4 information that shows (a) wiring of a signal line that requires  
5 tamper-resistance and (b) placement of components;

6 an exposed portion detecting means for referring to the  
7 board information and detecting portions of the signal line that  
8 are not covered by the components on outside layers; and



9 a warning means for outputting a warning indicating the  
10 portions detected by the exposed portion detecting means.

1 16. The design check apparatus of Claim 15 further  
2 comprising:

3 an inside layer uncovered portion detecting means for  
4 referring to the board information and detecting portions of  
5 the signal line in inside layers that are not sandwiched between  
6 components or sheets of foil placed on two outside layers when  
7 viewed from above or below in a vertical direction, wherein  
8 the warning means further outputs a warning indicating  
9 the portions detected by the inside layer uncovered portion  
10 detecting means.

1 17. The design check apparatus of Claim 16 further  
2 comprising:

3 an opposite layer uncovered portion detecting means for  
4 referring to the board information and detecting portions of  
5 the signal line that are wired on one outside layer and are not  
6 covered by components on another outside layer that is opposite  
7 to the outside layer when viewed from above or below in a vertical  
8 direction, wherein

9 the warning means further outputs a warning indicating

10 the portions detected by the opposite layer uncovered portion  
11 detecting means.

1 18. A design method for a multilayer board, the design  
2 method comprising:

3 a component information acquiring step for acquiring  
4 component information that shows (a) positions of circuit  
5 components, (b) sizes of the components, and (c) terminals  
6 contained by the components;

7 a tamper-resistant signal line specifying step for  
8 specifying a signal line that requires tamper-resistance, among  
9 signal lines connecting terminals;

10 an outside layer wiring setting step for referring to the  
11 component information and setting areas on outside layers covered  
12 by circuit components as outside layer wiring possible areas;

13 a via setting step for referring to the component  
14 information, detecting an area where a first outside area wiring  
15 possible area of one outside layer overlaps another outside area  
16 wiring possible area of a second outside layer that is opposite  
17 to the first outside layer, when viewed from above or below in  
18 a vertical direction, and sets the detected area as a via possible  
19 area; and

20 a wiring information generating step for determining a

21 wiring pattern so that signal lines requiring tamper-resistance  
22 are wired only in the outside layer wiring possible areas and  
23 the via possible area, and generating wiring information that  
24 shows the determined wiring pattern.

1 19. A design method for a multilayer board, the design  
2 method comprising:

3 a board information acquiring step for acquiring board  
4 information that shows (a) the number of layers and (b)  
5 ground/power-source layers;

6 a tamper-resistant signal line specifying step for  
7 specifying a signal line that requires tamper-resistance;

8 an inside layer wiring setting step for referring to the  
9 board information and setting layers sandwiched between two  
10 ground/power-source layers as wiring possible inside layers;  
11 and

12 a wiring information generating step for determining a  
13 wiring pattern so that signal lines requiring tamper-resistance  
14 are wired in the wiring possible inside layers, and generating  
15 wiring information that shows the determined wiring pattern.

1 20. A design method for a multilayer board, the design  
2 method comprising:

3           a board information acquiring step for acquiring board  
4 information that shows (a) wiring of signal lines that require  
5 tamper-resistance and (b) positions of components connected to  
6 the signal lines;

7           an exposed portion detecting step for referring to the  
8 board information and detecting portions of the signal lines  
9 that are not covered by the components connected to the signal  
10 lines on outside layers; and

11          a placement information generating step for determining  
12 a placement pattern so that one or more components that have  
13 not been placed yet are placed to cover the detected portions,  
14 and generating placement information that shows the determined  
15 placement pattern.

1           21. A design method for a multilayer board, the design  
2 method comprising:

3           a board information acquiring step for acquiring board  
4 information that shows (a) the number of layers and (b) wiring  
5 of signal lines;

6           a tamper-resistant signal line specifying step for  
7 specifying a signal line that requires tamper-resistance;

8           a plane layer detecting step for detecting, as plane layers,  
9 two layers that sandwich a layer on which the signal line is

10 wired; and

11 a placement information generating step for determining  
12 a placement pattern so that sheets of foil on the plane layers  
13 cover the wiring of the signal line sandwiched by the plane layers  
14 when viewed from above or below in a vertical direction, and  
15 generating placement information that shows the determined  
16 placement pattern.

1 22. A design check method for a multilayer board, the  
2 design check method comprising:

3 a board information acquiring step for acquiring board  
4 information that shows (a) wiring of a signal line that requires  
5 tamper-resistance and (b) placement of components;

6 an exposed portion detecting step for referring to the  
7 board information and detecting portions of the signal line that  
8 are not covered by the components on outside layers; and

9 a warning step for outputting a warning indicating the  
10 portions detected by the exposed portion detecting step.

1 23. A program for allowing a computer to design a  
2 multilayer board, the program comprising:

3 a component information acquiring step for acquiring  
4 component information that shows (a) positions of circuit

5 components, (b) sizes of the components, and (c) terminals  
6 contained by the components;  
7 a tamper-resistant signal line specifying step for  
8 specifying a signal line that requires tamper-resistance, among  
9 signal lines connecting terminals;  
10 an outside layer wiring setting step for referring to the  
11 component information and setting areas on outside layers covered  
12 by circuit components as outside layer wiring possible areas;  
13 a via setting step for referring to the component  
14 information, detecting an area where a first outside area wiring  
15 possible area of one outside layer overlaps another outside area  
16 wiring possible area of a second outside layer that is opposite  
17 to the first outside layer, when viewed from above or below in  
18 a vertical direction, and sets the detected area as a via possible  
19 area; and  
20 a wiring information generating step for determining a  
21 wiring pattern so that signal lines requiring tamper-resistance  
22 are wired only in the outside layer wiring possible areas and  
23 the via possible area, and generating wiring information that  
24 shows the determined wiring pattern.

1 24. A program for allowing a computer to design a  
2 multilayer board, the program comprising:

3 a board information acquiring step for acquiring board  
4 information that shows (a) the number of layers and (b)  
5 ground/power-source layers;

6 a tamper-resistant signal line specifying step for  
7 specifying a signal line that requires tamper-resistance;

8 an inside layer wiring setting step for referring to the  
9 board information and setting layers sandwiched between two  
10 ground/power-source layers as wiring possible inside layers;  
11 and

12 a wiring information generating step for determining a  
13 wiring pattern so that signal lines requiring tamper-resistance  
14 are wired in the wiring possible inside layers, and generating  
15 wiring information that shows the determined wiring pattern.

1 25. A program for allowing a computer to design a  
2 multilayer board, the program comprising:

3 a board information acquiring step for acquiring board  
4 information that shows (a) wiring of signal lines that require  
5 tamper-resistance and (b) positions of components connected to  
6 the signal lines;

7 an exposed portion detecting step for referring to the  
8 board information and detecting portions of the signal lines  
9 that are not covered by the components connected to the signal

10 lines on outside layers; and

11 a placement information generating step for determining  
12 a placement pattern so that one or more components that have  
13 not been placed yet are placed to cover the detected portions,  
14 and generating placement information that shows the determined  
15 placement pattern.

1 26. A program for allowing a computer to design a  
2 multilayer board, the program comprising:

3 a board information acquiring step for acquiring board  
4 information that shows (a) the number of layers and (b) wiring  
5 of signal lines;

6 a tamper-resistant signal line specifying step for  
7 specifying a signal line that requires tamper-resistance;

8 a plane layer detecting step for detecting, as plane layers,  
9 two layers that sandwich a layer on which the signal line is  
10 wired; and

11 a placement information generating step for determining  
12 a placement pattern so that sheets of foil on the plane layers  
13 cover the wiring of the signal line sandwiched by the plane layers  
14 when viewed from above or below in a vertical direction, and  
15 generating placement information that shows the determined  
16 placement pattern.



1           27. A program for allowing a computer to check a design  
2 of a multilayer board, the program comprising:  
3           a board information acquiring step for acquiring board  
4 information that shows (a) wiring of a signal line that requires  
5 tamper-resistance and (b) placement of components;  
6           an exposed portion detecting step for referring to the  
7 board information and detecting portions of the signal line that  
8 are not covered by the components on outside layers; and  
9           a warning step for outputting a warning indicating the  
10 portions detected by the exposed portion detecting step.

1           28. A recording medium recording a program for allowing  
2 a computer to design a multilayer board, the program comprising:  
3           a component information acquiring step for acquiring  
4 component information that shows (a) positions of circuit  
5 components, (b) sizes of the components, and (c) terminals  
6 contained by the components;  
7           a tamper-resistant signal line specifying step for  
8 specifying a signal line that requires tamper-resistance, among  
9 signal lines connecting terminals;  
10           an outside layer wiring setting step for referring to the  
11 component information and setting areas on outside layers covered  
12 by circuit components as outside layer wiring possible areas;

13 a via setting step for referring to the component  
14 information, detecting an area where a first outside area wiring  
15 possible area of one outside layer overlaps another outside area  
16 wiring possible area of a second outside layer that is opposite  
17 to the first outside layer, when viewed from above or below in  
18 a vertical direction, and sets the detected area as a via possible  
19 area; and

20 a wiring information generating step for determining a  
21 wiring pattern so that signal lines requiring tamper-resistance  
22 are wired only in the outside layer wiring possible areas and  
23 the via possible area, and generating wiring information that  
24 shows the determined wiring pattern.

1 29. A recording medium recording a program for allowing  
2 a computer to design a multilayer board, the program comprising:  
3 a board information acquiring step for acquiring board  
4 information that shows (a) wiring of signal lines that require  
5 tamper-resistance and (b) positions of components connected to  
6 the signal lines;

7 an exposed portion detecting step for referring to the  
8 board information and detecting portions of the signal lines  
9 that are not covered by the components connected to the signal  
10 lines on outside layers; and

11 a placement information generating step for determining  
12 a placement pattern so that one or more components that have  
13 not been placed yet are placed to cover the detected portions,  
14 and generating placement information that shows the determined  
15 placement pattern.

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